Design and simulation a three-phase inverter by the space vector pulse width modulation control method with the approach of reducing the output voltage total harmonic distortion

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ABSTRACT

Nowadays power quality is one of the most important aspects of power electronics engineering. In this article it is tried to reduce the power losses in power transmission in the presented three-phase inverter from the AC main to the load side with the space vector pulse width modulation method of switching the three-phase inverter in the controlling circuit unit. this article presents a three-phase inverter with a switching frequency of 10 KHZ. This three-phase inverter is controlled by the space vector pulse width modulation method of switching the power electronic switches of this inverter. This switching method of the inverter is helpful due to the reducing of the output voltage third total harmonic distortion. After the output voltage's third total harmonic distortion is reduced, we have a better output voltage waveform with lower third harmonic and higher power factor and a better power quality of the output signal; as a result, a better power transmission from the DC side of the inverter to the AC side and the least power losses is seen by using this controlling method.
Keywords: **SVPWM, THD, Power factor**

1. *INTRODUCTION*

This article presents a three-phase, four leg medium frequency inverter that is able to meet the needs of avionics and radar equipment that can maintain a stable three-phase output voltage under unbalanced load.[1] In this paper a three-phase inverter is designed and presented on the base of LabVIEW FPGA module for the simulation platform with the SVPWM method of modulation for the three-phase inverter. Results show that the output waveform of the inverter is stable, less harmonic, the amplitude and frequency of the output voltage and the switching frequency is adjustable.[2] In this paper first a model for Space vector PWM is made and simulated using MATLAB/SIMULINK software and its performance is compared with Sinusoidal PWM. The simulation study reveals that Space vector PWM utilizes dc bus voltage more effectively and generates less THD when compared with sine PWM.[3] This article introduced SVPWM control technology into three-phase grid-connected inverter, created a main circuit mathematical model of three-phase grid connected inverter and detailed the implementation of SVPWM modulation method with MATLAB software.[4] This paper further analyzes the intrinsic relationship between the common mode voltage and the zero-sequence voltage of three-phase three-leg three-level inverters, with a novel SVPWM method proposed. The presented algorithm makes the zero-sequence voltage impulse periodically balanced by using the small voltage vectors reasonably. Compared with the traditional SVPWM scheme, the proposed method can remarkably reduce the common mode voltage magnitude over all frequency.[5]

1.1 Main discussion

1.1.1 Three – phase inverter circuit

In this step it is focused on the body of the three-phase inverter which has three legs and six IGBT's that transfers a 700 V DC voltage to an AC voltage with a 380 V amplitude on 50 HZ frequency with low THD of output voltage waveform. In order to achieve to this, aim an SVPWM method of switching the IGBT's is used which is presented and discussed in the next part. In the figure 1 the main three-phase inverter is shown.

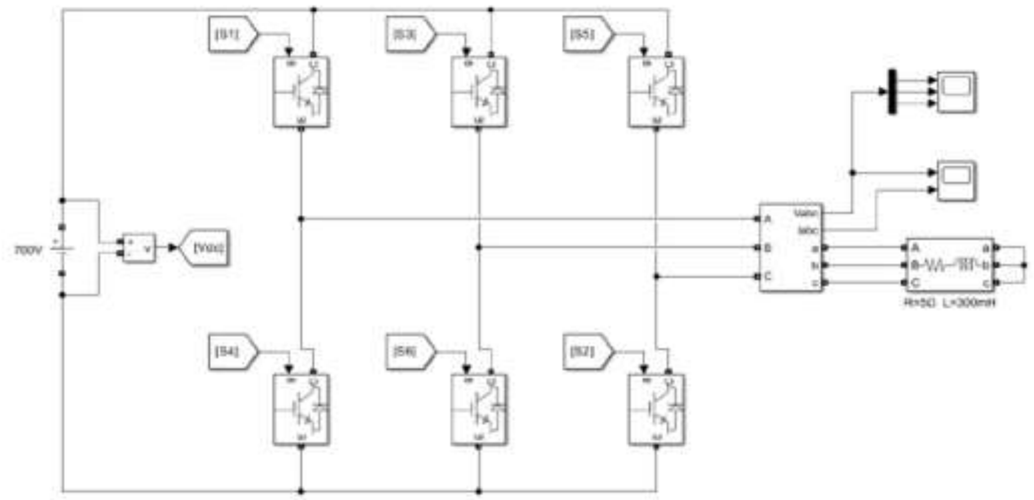

Fig. 1. *Three-phase inverter with RL load*

In the figure 1 an RL load is used in order to produce the desired output voltage. In order to preventing the output voltage being short circuit when one of IGBT's in a leg is on the next IGBT in the same leg must be off. Let the load resistance and inductance be setup on 5 ohm and 300 mH respectively. In this case the produced SVPWM pulses are compared with a sawtooth waveform with the desired switching frequency. After that the desired output waveforms are fed to the IGBT's gates for being controlled.

1.1.2 Control circuit

According *In the figure 2 the control circuit of the three-phase inverter is shown and presented. As it is discussed this control circuit is based on SVPWM method*.

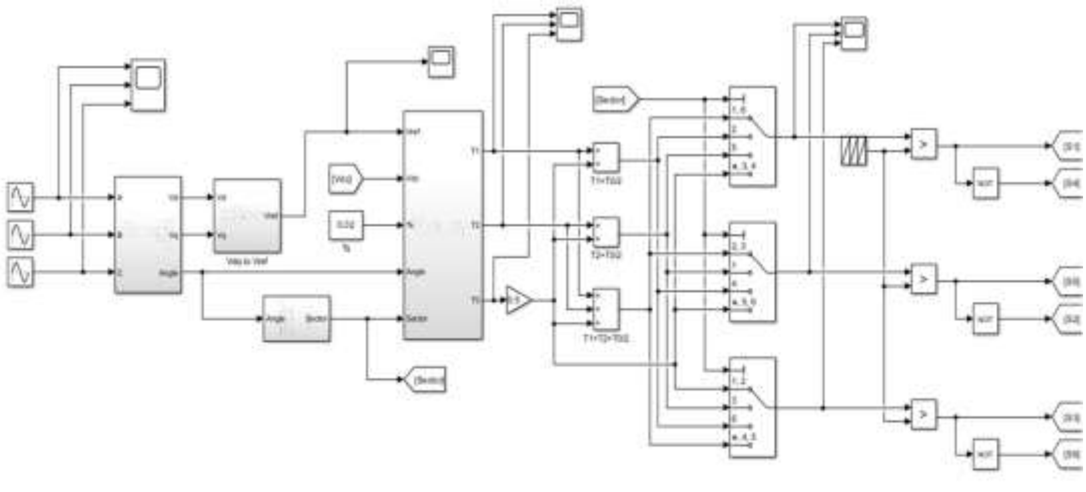

Fig.2. Control circuit based on SVPWM method

According to the figure 2 three different input voltages with the same amplitude and 120 degrees phase difference is transferred from abc-reference to the dq-reference with Clark transformation. This is done by the module bellow:

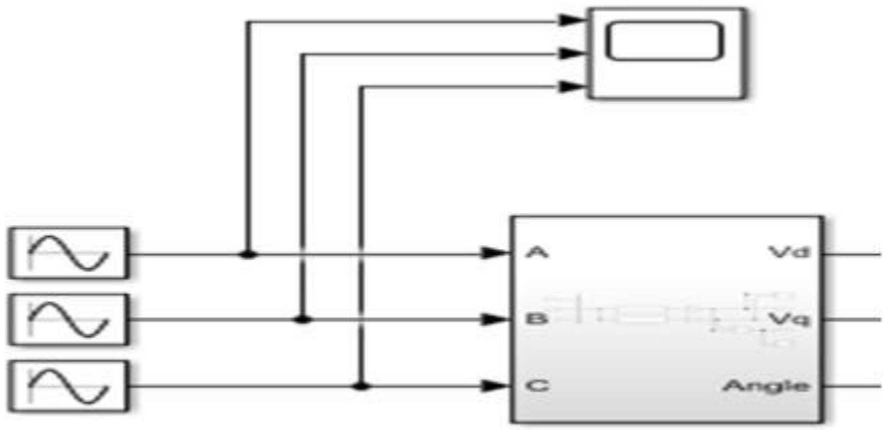

Fig.3. The module of Clark-transformation connected to the three-phase input voltage

Clark-transformation module is as follows:

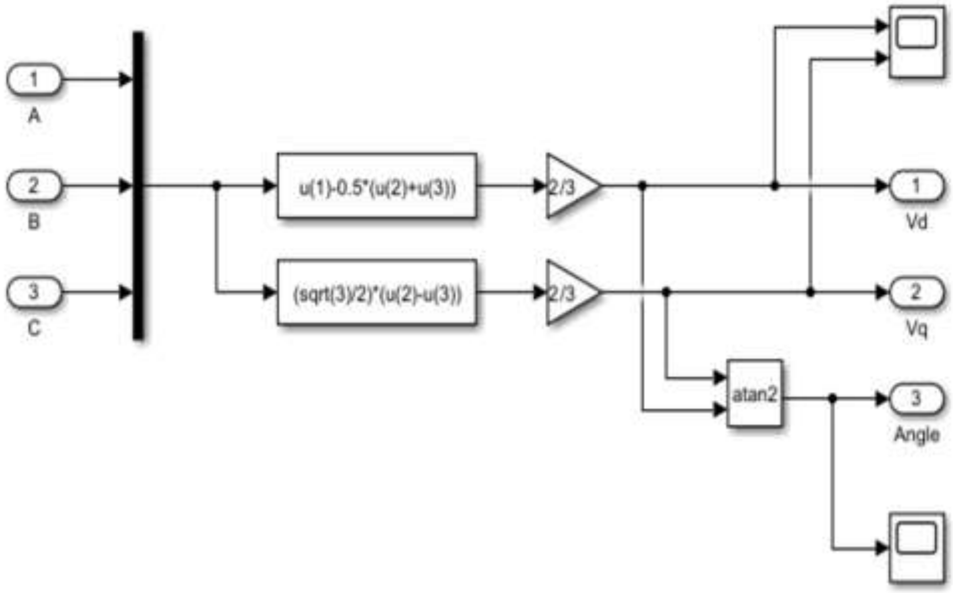

Fig.4. Clark-transformation module

After transforming the abc-reference voltages to dq-reference voltages the reference voltage is produced with the module bellow:

Fig.5. The module of generating the reference voltage from dq-reference voltage

The figure fifth's math relations is as follows:

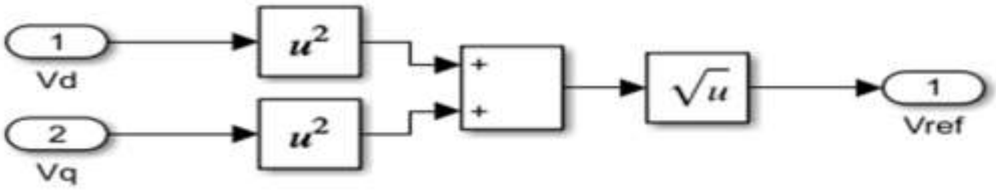

Fig.6. The math relations in the module of figure number 5

In the figure 7 the angle is transferred from degrees to radian:

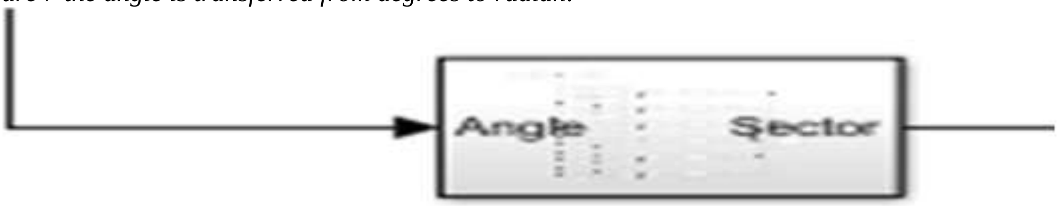

Fig.7. The module of transferring the angle from degrees to radian

The module of figure number 7 is works as it is shown in the figure number 8:

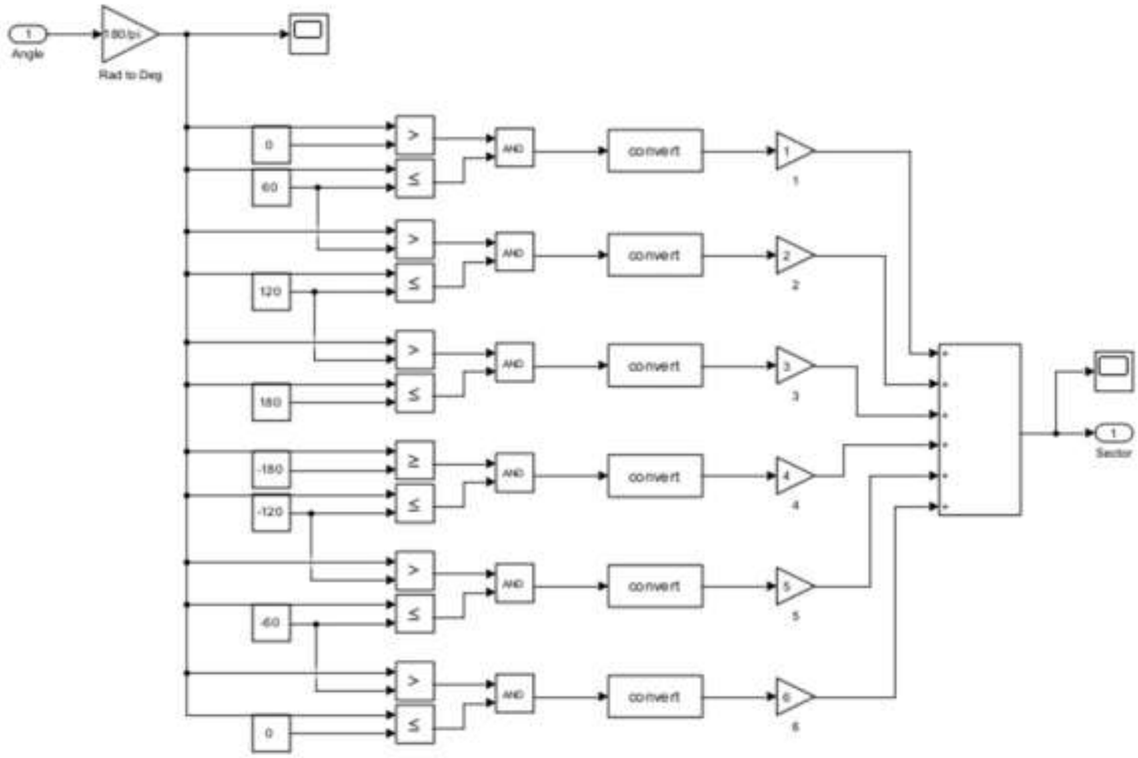

Fig.8. The module of transferring the angle from degrees to radian

The sectors of space vectors are shown in the figure number 9:

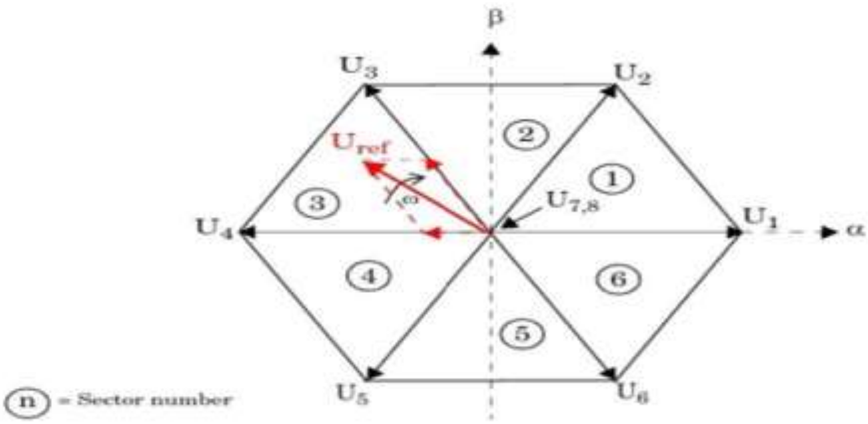

Fig.9. The sectors of space vector

As it is shown in figure number 9 there are six sectors with 60 degrees. After transferring the angle to degrees these angles are compared with these sectors in order to relating each of these angles to their related sectors. In the output, a gain is defined for each region to generate the pulse corresponding to the desired angles of the reference voltage. The block diagram of calculating the T0, T1 and T2 is as follows:

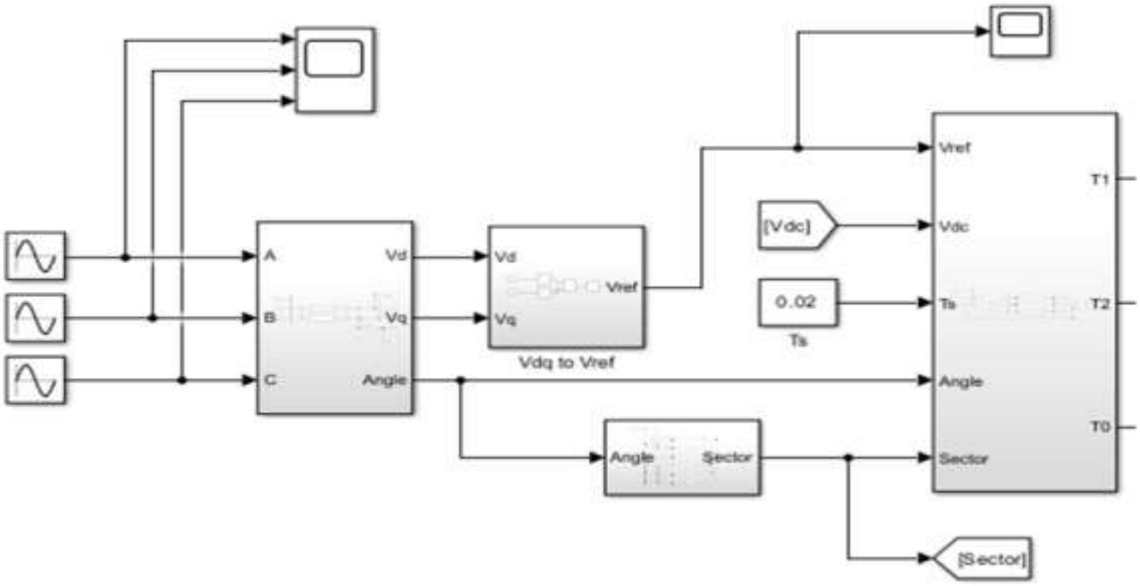

Fig.10. The block diagram of calculating the T0, T1 and T2

According to the figure 10, the T0, T1 and T2 are generated from Vref, Vdc, Ts, angles and sectors with the math relation that is shown in figure 11:

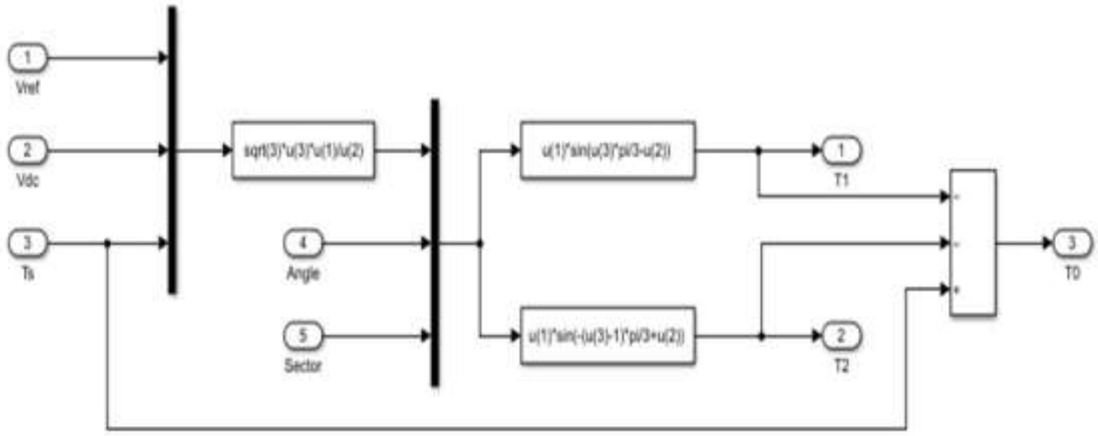

Fig.11. The math relations between Vref, Vdc, Ts, Angles, sectors and T0, T1, T2

In the next step by using the SVPWM switching pattern and according to T0, T1 and T2 the switching pulses are generated as bellows:

Switches 2, 4, 6 (Switches bellow)	Switches 1, 3, 5 (Switches above)	Sectors
S2=T0/2+T1+T2 S4=T0/2 S6=T1+T0/2	S1=T1+T2+T0/2 S3=T2+T0/2 S5=T0/2	1
S4=T2+T0/2 S6=T0/2 S2=T1+T2+T0/2	S1=T1+T0/2 S3=T1+T2+T0/2 S5=T0/2	2
S4=T1+T2+T0/2 S6=T0/2 S2=T1+T0/2	S1=T0/2 S3=T1+T2+T0/2 S5=T2+T0/2	3
S4=T1+T2+T0/2 S6=T2+T0/2 S2=T0/2	S1=T0/2 S3=T1+T0/2 S5=T1+T2+T0/2	4
S4=T1+T0/2 S6=T1+T2+T0/2 S2=T0/2	S1=T2+T0/2 S3=T0/2 S5=T1+T2+T0/2	5
S4=T0/2 S6=T1+T2+T0/2 S2=T2+T0/2	S1=T1+T2+T0/2 S3=T0/2 S5=T1+T0/2	6

Table.1. The switching pattern of SVPWM method

After that with the help of a multiport switch the state of switching in each sector is cleared as follows:

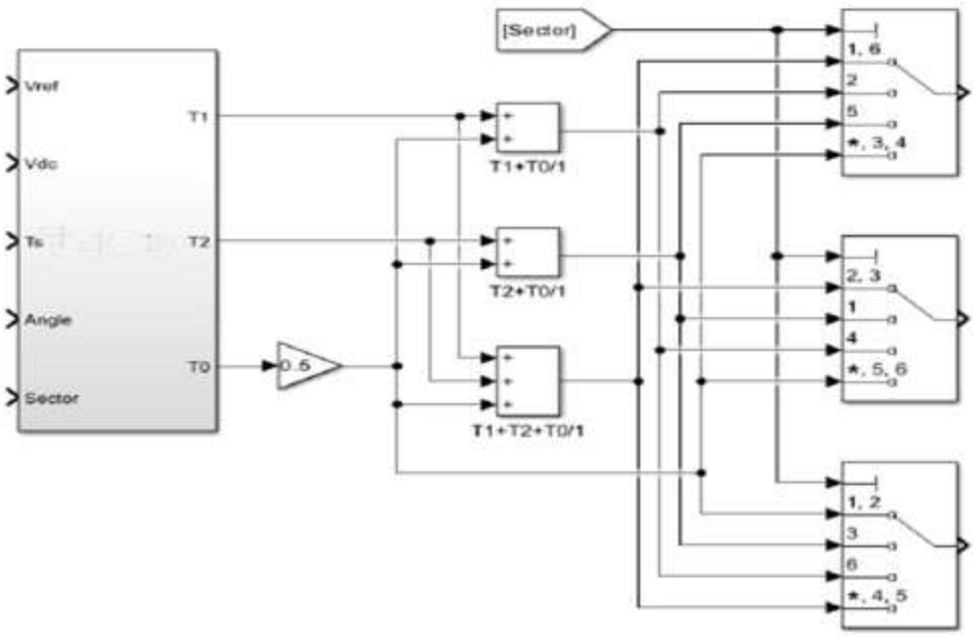

Fig.12. The switching state in each sector

In the end as it is discussed the output SVPWM waveform is compared with a triangular waveform with the switching frequency and then the required pulses for each switch is generated and fed to each IGBT.

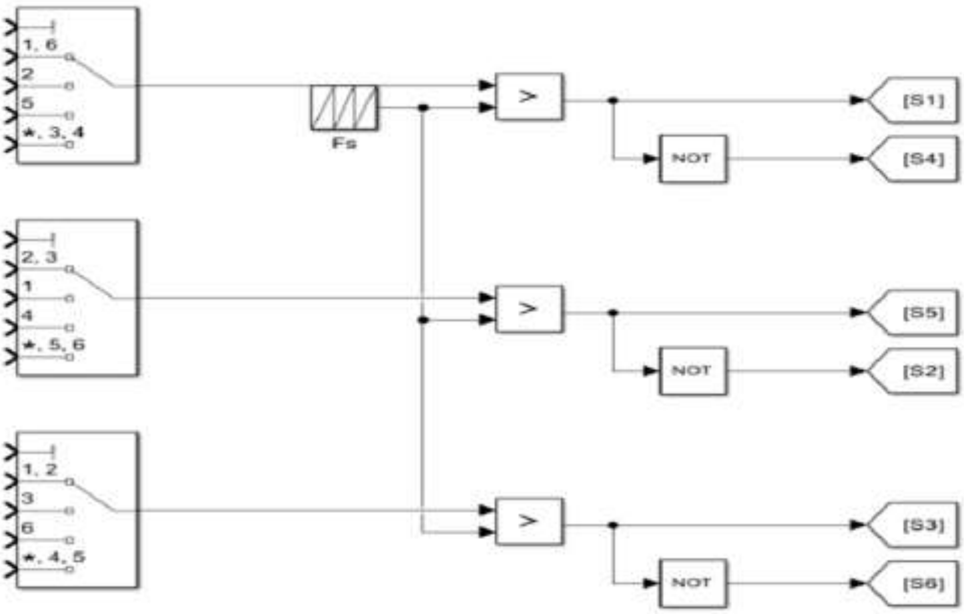

Fig.13. The required pulses for each switch of three-phase inverter

2.1 Simulation results

In this section the output voltages and currents waveform and the output voltage's THD shown by MATLAB software. Let the switching frequency be 10 KHZ.

The abc-voltage waveforms are as follows:

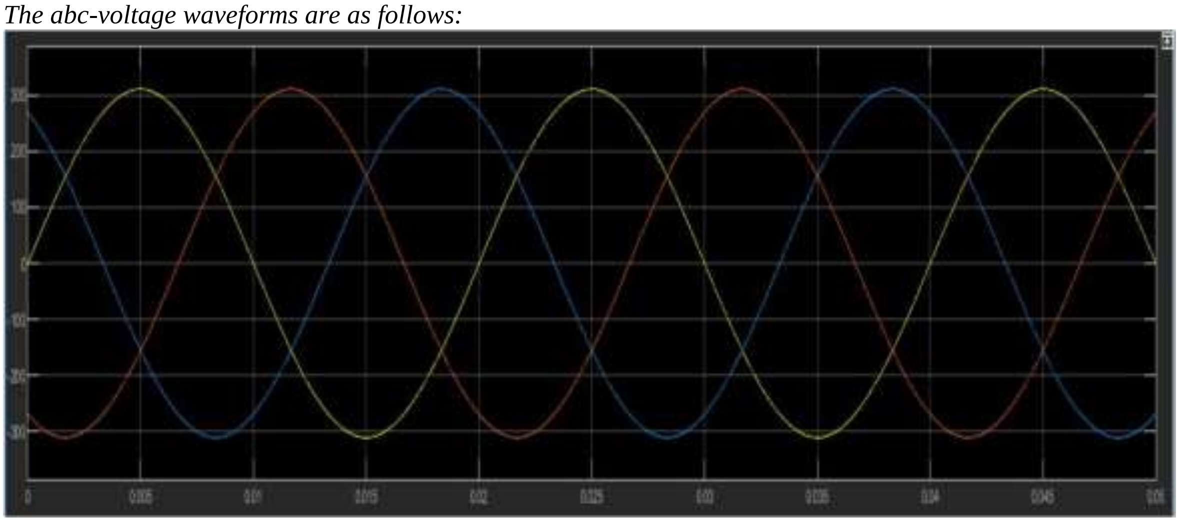

Fig.14. The abc-voltage waveform

The waveform of T1 is as follows:

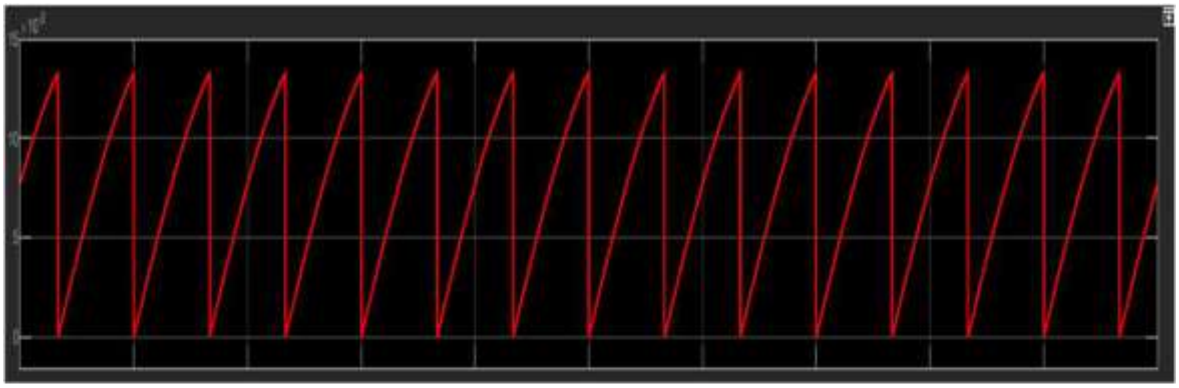

Fig.15. The waveform of T1

The waveform of T0 is as follows:

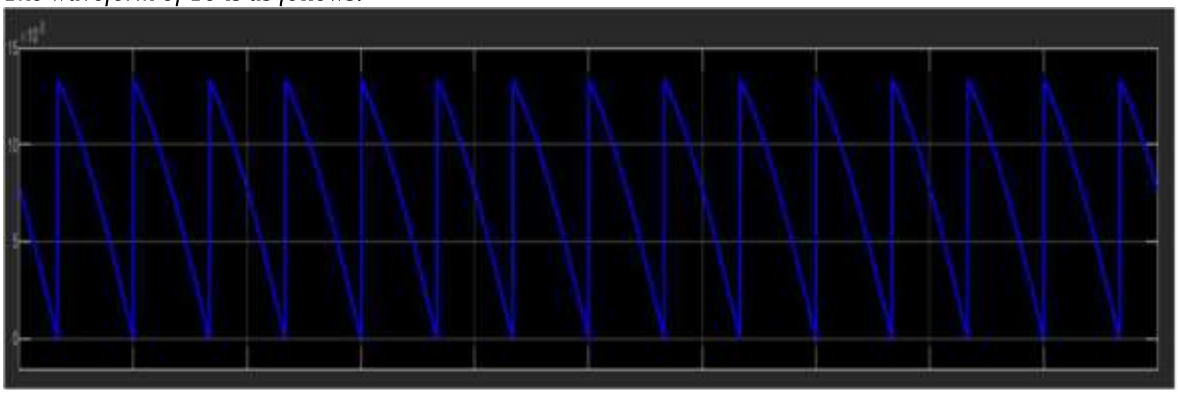

Fig.16. The waveform of T0

The waveform of T2 is shown as follows:

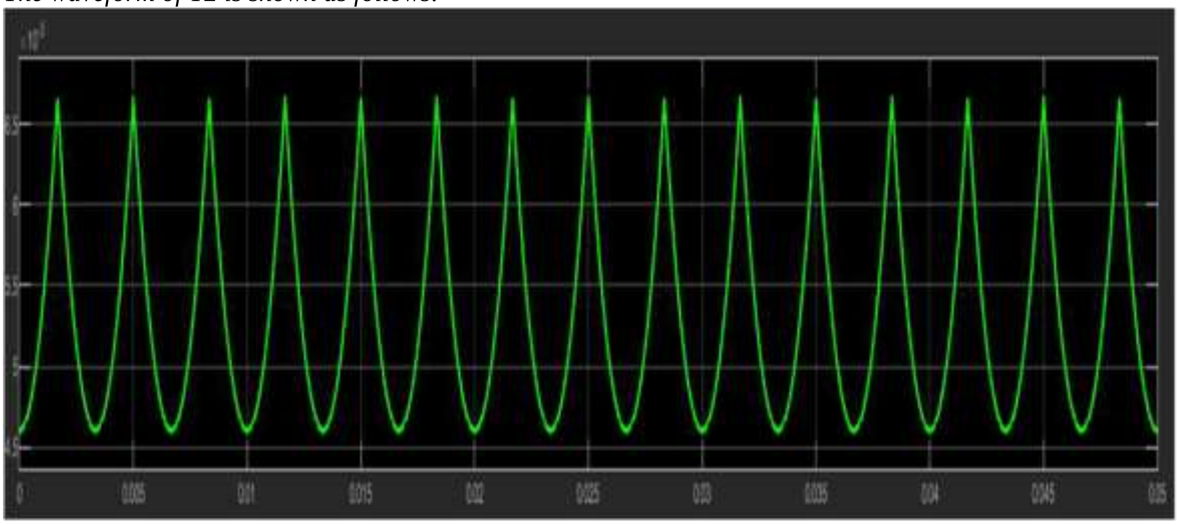

Fig.17. The waveform of T2

The SVPWM waveforms are shown as follows:

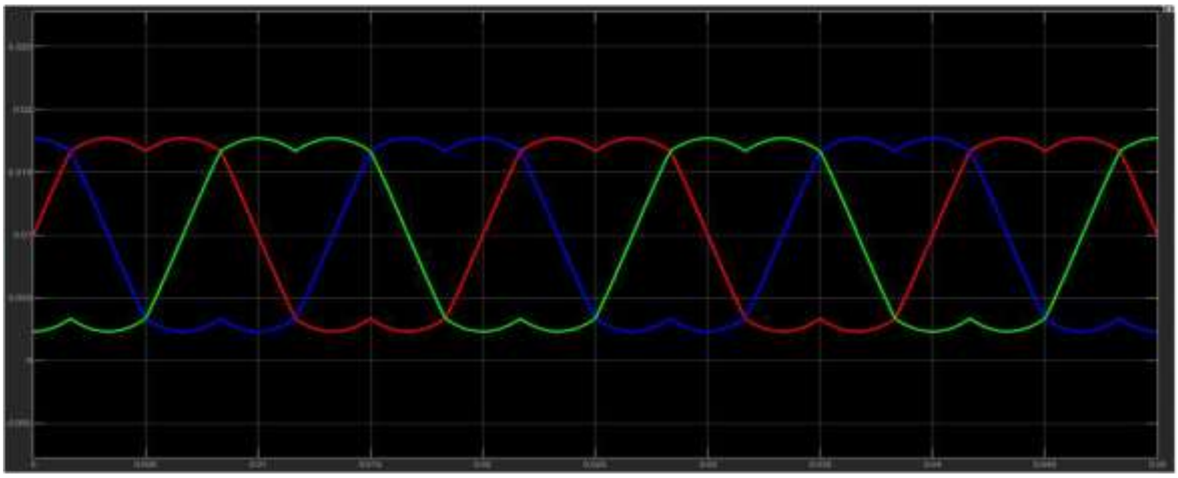

Fig.18. The SVPWM waveforms

The output voltage waveforms are shown as follows:

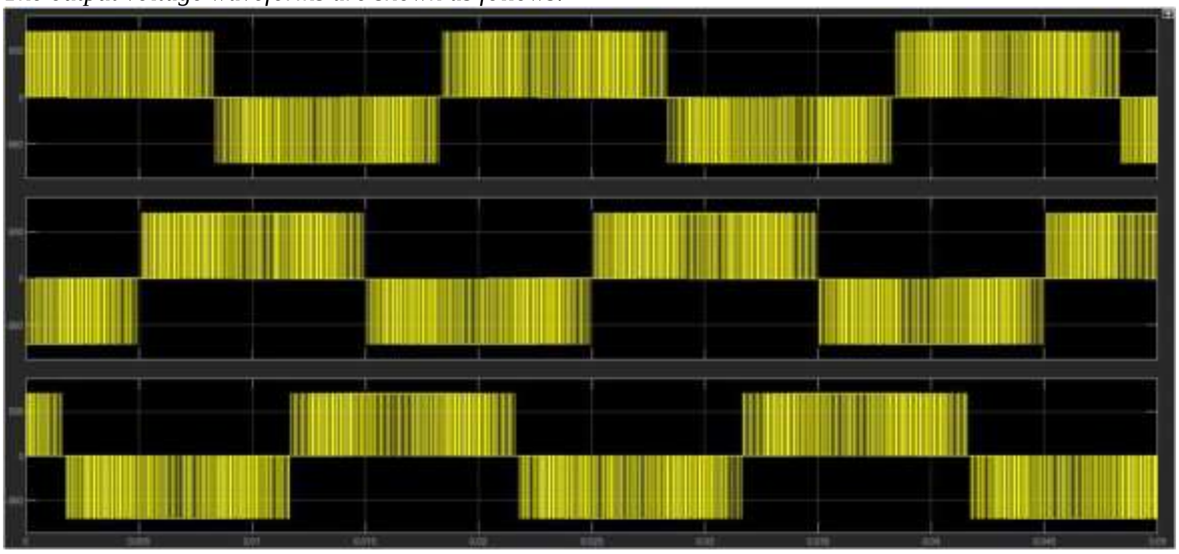

Fig.19. The output voltage waveforms

The THD of phase a of output voltage waveforms are calculated and shown as follows:

Sampling time	=	1e-06 sec.	
Samples per cycle	=	20000	
DC component	=	0.108	
Fundamental	=	539.7 peak (381.6 rms)	
THD	=	0.34%	

0 Hz	DC	0.02%	270.0°
25 Hz	---	0.00%	185.1°
50 Hz	Fnd	100.00%	209.9°
75 Hz	---	0.00%	180.8°
100 Hz	h2	0.02%	-13.8°
125 Hz	---	0.00%	180.6°
150 Hz	h3	0.09%	221.5°
175 Hz	---	0.00%	181.6°
200 Hz	h4	0.08%	135.1°
225 Hz	---	0.00%	180.8°
250 Hz	h5	0.03%	-86.6°

Fig.20. The THD of phase a of output voltage waveform

The THD of phase b of output voltage waveforms are shown as follows:

Sampling time	=	1e-06 sec.
Samples per cycle	=	20000
DC component	=	0.2098
Fundamental	=	538.8 peak (381 rms)
THD	=	0.33%

0 Hz	DC	0.04%	90.0°
25 Hz	---	0.00%	182.5°
50 Hz	Fnd	100.00%	270.0°
75 Hz	---	0.00%	185.0°
100 Hz	h2	0.01%	90.0°
125 Hz	---	0.00%	183.9°
150 Hz	h3	0.12%	269.9°
175 Hz	---	0.00%	175.9°
200 Hz	h4	0.12%	269.9°
225 Hz	---	0.00%	182.1°
250 Hz	h5	0.06%	269.9°

Fig.21. The THD of phase b of output voltage waveform

The THD of phase c of output voltage waveforms are shown as follows:

Sampling time = 1e-06 sec.
Samples per cycle = 20000
DC component = 0.1013
Fundamental = 539.7 peak (381.6 rms)
THD = 0.34%

0 Hz	DC	0.02%	270.0°
25 Hz	---	0.00%	5.9°
50 Hz	Fnd	100.00%	150.0°
75 Hz	---	0.00%	2.2°
100 Hz	h2	0.02%	193.7°
125 Hz	---	0.00%	1.4°
150 Hz	h3	0.09%	138.4°
175 Hz	---	0.00%	0.7°
200 Hz	h4	0.08%	44.7°
225 Hz	---	0.00%	0.9°
250 Hz	h5	0.03%	86.4°

Fig.22. The THD of phase c of output voltage waveform

3.1 Conclusion

SVPWM method of switching IGBTs in a three-phase inverter is one of the best ways for reducing THD in the output voltage waveform in power electronics engineering. In this paper by using this method of switching IGBTs in 10 KHZ of switching frequency the THD of each output voltage waveform phases will be reduced to less than 0.4% as a result the output power quality will be improved. By reducing the THD of output voltage, the output power factor will become better and higher therefore the power transmission from the DC side of the inverter to the AC side of it will be improved with the least value of power losses.

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